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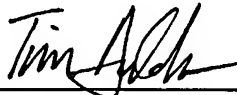
Applicant further reserves the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any additional fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: November 5, 2004

By:  Reg. No. 43,592 for:
David W. Hill
Reg. No. 28,220

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Application Number
Filing Date
First Named Inventor
Art Unit
Examiner Name
Attorney Docket Number

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Sheet	1	of	1
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Examiner Initials	Cite No. ¹	Document Number	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation ⁶
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Examiner Initials ¹	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation ⁶
		YUTAKA ARIMA, "Higher Integration of Neural Network with Learning Function," Study of Associative Memory Analog Neural Network LSI with Learning Function (January 1998).	✓
		"Chaos and Associative Memory," Computer Today (July 1999).	✓
		YUTAKA ARIMA, et al., "A Self Learning Neural Network Chip with 125 Neurons and 10K Self-Organization Synapses," 26 IEEE Journal of Solid-State Circuits 607 (April 1991).	
		YUTAKA ARIMA, et al., "A 336-Neuron, 28K-Synapse, Self-Learning Neural Network Chip with Branch-Neuron-Unit Architecture," 26 IEEE Journal of Solid-State Circuits 1637 (November 1991).	
		YUTAKA ARIMA, et al., "A Refreshable Analog VLSI Neural Network Chip with 400 Neurons and 40K Synapses," 27 IEEE Journal of Solid-State Circuits 1854 (December 1992).	

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